What is claimed is:

1. A bus performance evaluation method for algorithm description in which evaluation is performed on performance of a bus interconnecting between hardware and software by using sources described by a general purpose high-level language for verification of an algorithm, said bus performance evaluation method comprising the steps of:

modifying the sources by executing a specific evaluation function when data transfer is caused on the bus; and

in response to modified sources, structuring a simulation platform for use in an architecture design.

2. A bus performance evaluation method for the algorithm description according to claim 1 further comprising the step of:

performing simulation using the simulation platform to allow calculation of bus traffic for a processing rate of the bus, so that the evaluation of the performance of the bus is performed at a high-level stage of design.

3. A bus performance evaluation method for the algorithm description according to claim 1 or 2 further comprising the step of:

feeding back result of the evaluation of the performance of the bus to the sources used in the verification of the algorithm, so that the architecture design is performed at a high-level stage of design.

4. A bus performance evaluation method for algorithm description in which

evaluation is performed on performance of a bus interconnecting between hardware and software by using sources described by a general purpose high-level language for verification of an algorithm, said bus performance evaluation method comprising the steps of:

structuring a simulation platform for use in an architecture design by using the sources;

performing the evaluation of the performance of the bus by using the simulation platform;

modifying the sources in response to result of the evaluation of the performance of the bus;

restructuring the simulation platform in response to the modified sources; and

performing the evaluation again on the performance of the bus by using the restructured simulation platform.

5. A bus performance evaluation method for the algorithm description according to claim 4 wherein structuring the simulation platform for use in an architecture design using the sources comprises the steps of:

analyzing the sources by prescribed units respectively to isolate a hardware portion and a software portion;

creating an evaluation function for counting bus traffic of the bus; and

effecting syntax correction on the sources by executing the evaluation function every time data transfer is caused on the bus.

6. A bus performance evaluation method for the algorithm description according to claim 4 wherein the evaluation is performed on the performance of the bus by using

the evaluation function, so that in response to the bus traffic that is finally produced with respect to the processing rate of the bus, isolation of the hardware and software is optimized.

7. A bus performance evaluation method for algorithm description in which evaluation is performed on performance of a bus interconnecting between hardware and software by using sources described by a general purpose high-level language, said bus performance evaluation method comprising the steps of:

creating an evaluation function for counting bus traffic of the bus;

sequentially reading in the sources line by line while effecting syntax analysis;

making a determination as to whether description of the sources represent writing data to variables that are defined in advance and are loaded onto the bus to be evaluated;

upon the determination, modifying the sources by using the evaluation function that is embedded just before or just after the variable to which the data is written;

repeating the foregoing steps until the sources are completely read in and modified up to a last line;

structuring a simulation platform for use in an architecture design by compiling the sources being modified;

performing calculation on the bus traffic for the bus by executing the simulation platform;

producing the bus traffic with regard to a processing rate of the bus that is already known; and

performing the evaluation on the performance of the bus in response to the bus traffic being produced.

8. A bus performance evaluation method for the algorithm description according to claim 7 wherein the variables loaded onto the bus consist of n bits while the bus consists of m bits (where n, m are both integral numbers, and $n \leqq m$), so that the bus traffic for the processing rate is produced such that a number of times in effecting data transfer on the bus is multiplied by n/m and is then divided by the processing rate.

9. A bus performance evaluation method according to any one of claims 1, 4 and 7 wherein the general purpose high-level language is C language or C++ language.

10. A bus performance evaluation method according to any one of claims 1, 5 and 7 wherein the evaluation function is to increment a pre-defined variable loaded onto the bus.